Getting Started with FPGAs

Digital Circuit Design, Verilog, and VHDL for Beginners

by Russell Merrick

errata updated to print 1

Page	Error	Correction	Print corrected
38	It also occurs on the **fifth** line of the truth table, so we can fill those in with a 1.	It also occurs on the **sixth** line of the truth table, so we can fill those in with a 1.	Pending
117	On the read side, the `i_Rd_En` and **`i`**`_Rd_DV` signals similarly communicate when we wish to read data . . .	On the read side, the `i_Rd_En` and **`o`**`_Rd_DV` signals similarly communicate when we wish to read data . . .	Pending
174 (ebook only)	When this happens we transition to the **`PATTERN _SHOW`** . . .	When this happens we transition to the **`PATTERN_SHOW`** . . .	Pending
208 (ebook only)	For example, 100010 100 becomes 011101 100.	For example, 100010**100** becomes 011101**100**.	Pending
Back cover	The book I wish had	The book I wish **I** had	Pending